Design and Simulation of 1-bit Sigma Delta ADC in 0.18um CMOS Technology

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ABSTRACT

This paper presents the design of a first order single bit Sigma-Delta ADC which is realized using CMOS technology. In this paper, a first Order Sigma-Delta ADC is implemented in a standard 0.18um CMOS technology. The Design and Simulation of the Modulator is done using Mentor Graphics Tool.

First order single bit Sigma Delta ADC Modulator is implemented using ±1.8 power supply and simulation results are plotted using Mentor Graphics Tool. This paper firstly elaborate about ADC types and Classification among Nyquist rates and Oversampling ADCs. Further, design of 1-bit Sigma Delta ADC is to be proposed which consists of Op-amp as a key component in Sigma delta ADC. Op-amp at integrator stage is with Gain Bandwidth (GB) is 5MHz, output resistance is 10KΩ, and power dissipation is 2.806 mW.

Keywords

CMOS Technology, Comparator, Mentor Graphics Tool, Op-Amp.

1. INTRODUCTION

For many years, the technique of sigma delta conversion is existence, and their use is becoming widespread. The application of these converters have been found in communications systems, industrial weight scales, precision measurement devices and professional audio. The sigma-delta (Σ-Δ) ADC is found in many applications where high resolution, low cost, low power, ADC is required. DSP technique is used in oversampling converters instead of analog converters which ultimately gives scope in order to improve resolution as compared to Nyquist rate converters. Sigma Delta ADC, a type of oversampling ADC is highly tolerant to analog circuit imperfections, thus making it a good choice to realize embedded ADC interfaces in modern systems-on-chip (SoCs).

A sigma-delta ADC comprises of an analog block of modulator and a digital block of decimator. The use of modulator is done in order to sample input signal at oversampling rate which generates a output stream of 1 bit.

For actual DSP decimator or down sampler is used as a digital filter. The decimator which is a crucial part of a sigma-delta ADC converts this one bit stream from modulator to a N bit stream according to resolution of ADC, Which also increases the final output resolution of the ADC.

In this project work we are going to design of Op-amp, Comparator and DAC for Sigma-Delta Analog–to-Digital Converter (ADC) using Mentor Graphics tool. The paper is being divided into five sections. In section 2,Basic of ADCs and types of ADCs. In section 3, designing of the Op-amp, Comparator and DAC. In section 4, Simulation results are presented. Finally in section 5, Conclusion.

2. BASIC OF ADCs

2.1. Ideal Analog and Digital Converter

The Analog to digital converter (ADC or A/D converter) has the opposite function as that of Digital to Analog converter and converts an analog input signal to a digital output signal, as shown in Figure.3

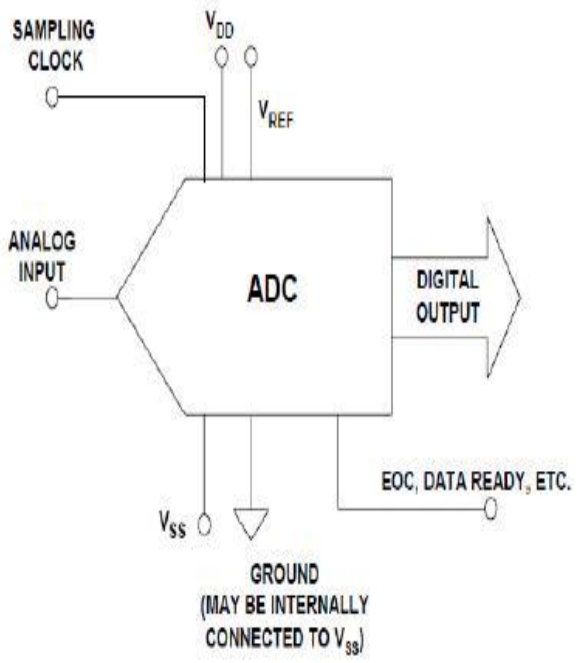

Fig.1 Ideal Block Diagram of Digital to Analog Converter[3]

where Bout is the digital output world while Analog Input and Vref are the analog input and reference signal respectively. Also, we define VLSB to be the signal change corresponding to a signal LSB change in the D/A case.

2.2 Types of ADC's

A. Nyquist-Rate ADCs

- Flash ADCs
- Sub-Ranging ADCs
- Folding ADCs
- Pipelined ADCs
- Successive Approximation (Algorithmic) ADCs
- Integrating (Serial) ADCs

B. Oversampling ADCs

- Delta-Sigma based ADCs

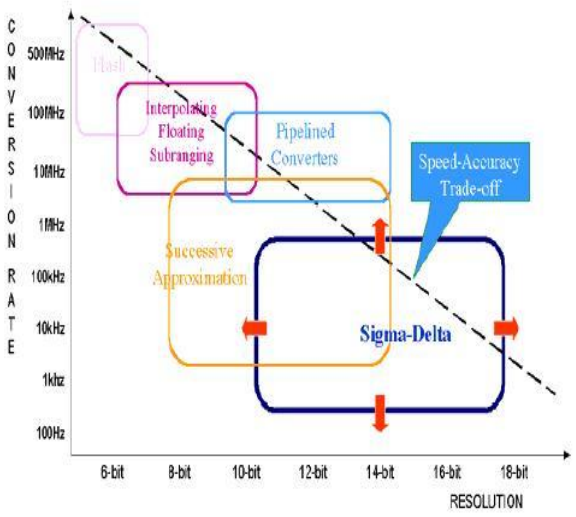

Fig. 2 Comparison of all ADCs according to specification of ADC[4]

TABLE I: Comparison of Different Types of ADC on the basis of Different Characteristics[4]

Characteristics	Flash	Pipelined	SAR	Sigma-delta
Throughput	High	Moderate	Small	Small
Resolution	8 bit	12-16 bit	10-16	>16 bits
Speed	250 Gsps	80 Msps	250 Ksps	> 200Ksps
Die size	Very small	Large	Small	Very large
Power	High	Moderate	Moderate	Low
Circuit complexity	Very simple	Moderately complex	Simple	Complex

2.3 Delta Sigma A/D Converter

This class of A/D converter stands out to be the most advanced, among all the Data converters discussed so far. A block level schematic of a first order A/D converter is as depicted below.

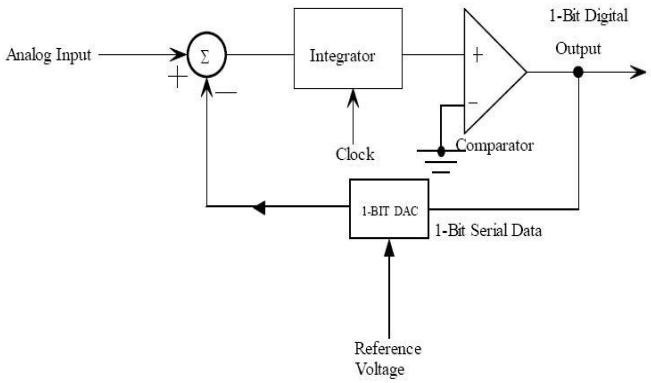

Fig.3 1 bit sigma delta ADC Block Diagram[3]

Figure shows the block diagram of a proposed first order Delta-sigma Converter (Σ-Δ ADC). It consists of Integrator, a comparator (1 bit ADC), 1-bit DAC. In above circuitry a 1-bit ADC (generally known as a Comparator), drive it with the output of an integrator, and feed the integrator with an input differenced with the output a 1-bit DAC.

The type of A/D converters discussed so far are Nyquist converters where by sampling rate is twice the input signal frequency for error free signal approximation. Only way to decrease the Quantization noise or better signal representation is sampling the signal many more times. This is the fundamental theory in sigma delta data converters.

3.DESIGN OF SIGMA DELTA ADC

3.1 Op-amp Design

The operational amplifier that the integrator uses must have the high gain to effectively carry out a smooth integration as well as a large enough bandwidth to support the high frequency sine waves it will be integrating. The op amp operates at the clock frequency, since the differences are being integrated over the region of time. Therefore, the gain bandwidth product of the op-amp must be greater than one at the clock frequency to effectively pass the signal. The amplifier used is shown in figure. The key thing to note to about the amplifier is the frequency compensation network which is used to push the high frequency zero out of the pass band of the op-amp[3].

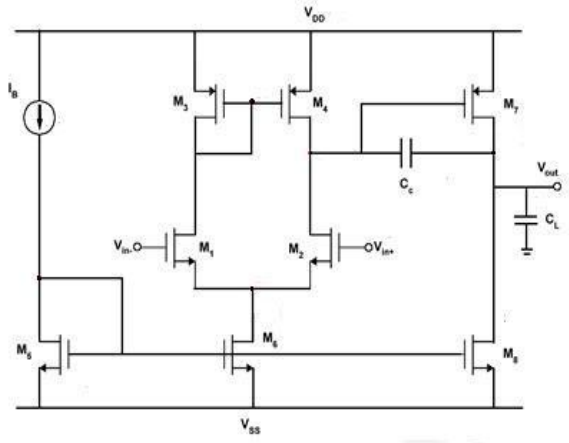

Fig. 4 Op-amp Design using CMOS

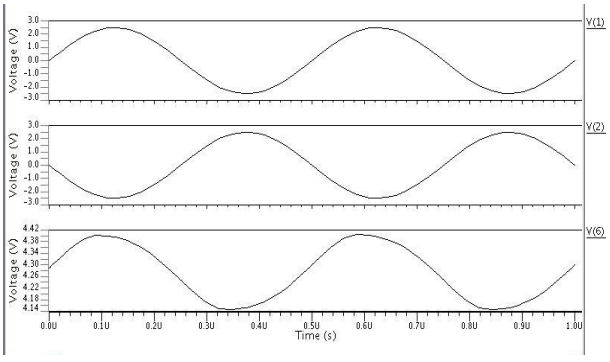

Fig.5 Op-amp Output

3.2 Design of Comparator

The 1- bit Sigma Delta consists of a 1-bit ADC which is composed of a comparator and a D-flip-flop. The design of

comparator is similar enough to that of an Op-amp .The only difference is the use of the compensation network consists of resistor and capacitor and extra multipliers on a biasing NMOS device. The comparator does not need the compensation network because its only function is to switch from rail to rail. Stability is not needed as it will only slow down the switching speed. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail [3].

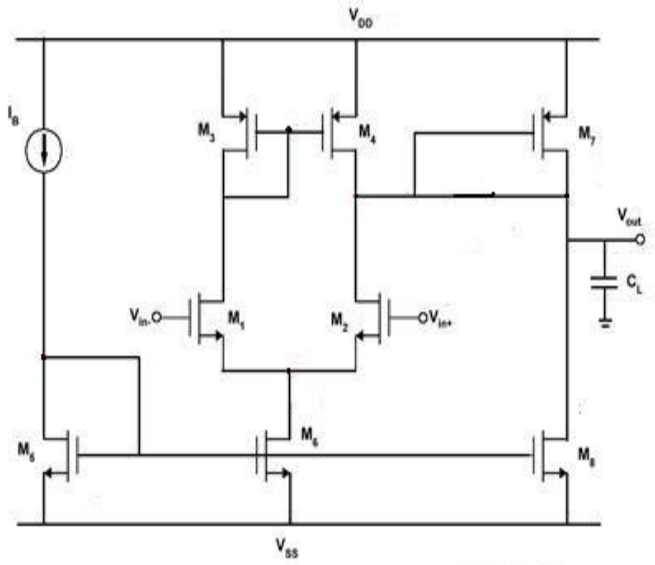

Fig.6 Comparator CMOS Design

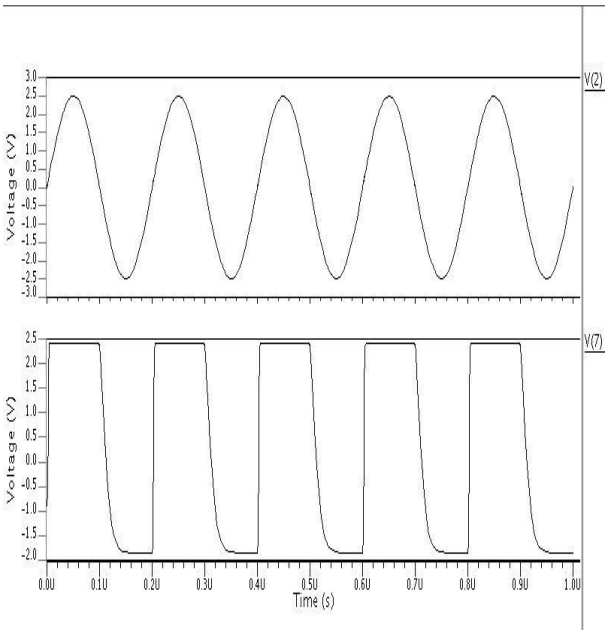

Fig.7 Comparator Output

3.3 Design of DAC

This DAC converts the 1-bit digital to an analog signal and fed back to the integrator again as shown in the block diagram of first order modulator of Fig.3. Fig.8 shows the circuit level diagram of 1-bit DAC. As the number of bits is only 1-bit, the corresponding analog output will also have two levels and similar to the digital output. The present 1-bit digital-to-analog converter has two reference voltages as shown in Fig.8, a positive reference voltage of +VREF and a negative reference voltage of – VREF [6].

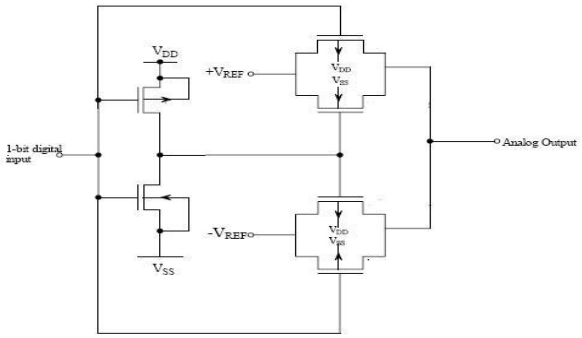

Fig. 8 Circuit Diagram of DAC

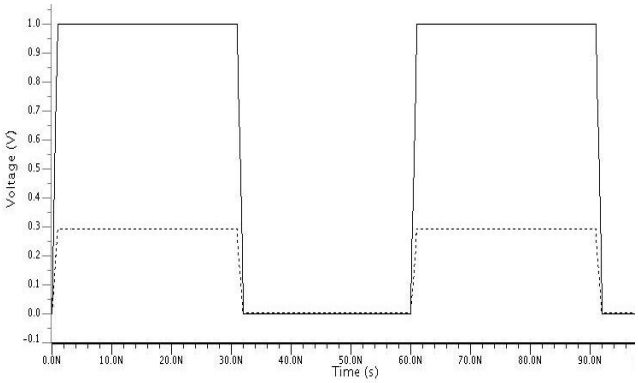

Fig.9 DAC Output

4. Simulation Result

The circuit design of Op-amp, Comparator and DAC for first order Sigma -Delta (Σ-Δ ADC) have been developed and implemented by using 0.18um CMOS Technology.

The whole First order Sigma-Delta ADC subsystem works very well under the following conditions.

Input sine wave frequency up to 5MHz.

Supply Voltage ±1.8V

Power Dissipation is 2.806mW.

Op-amp Gain is 60dB.

The output signal of converter is a pulse density waveform Figure 10 and 11 shows the input and output of (Σ-Δ) ADC modulator.

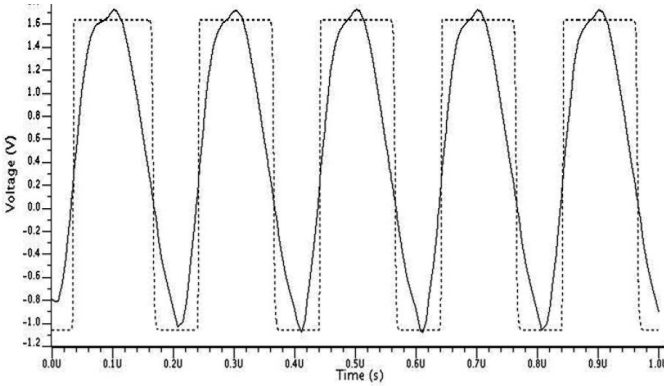

Fig.10 Output of Op-amp and Comparator

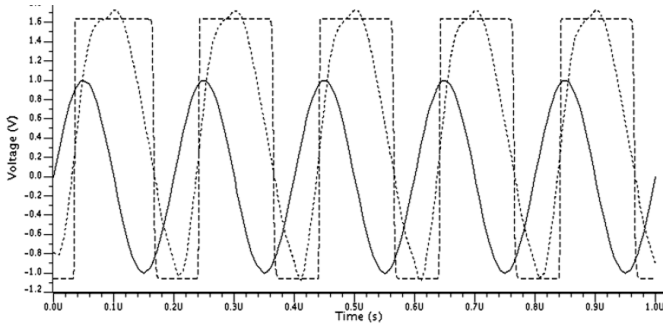

Fig 11 Combine waveform of input, Op-amp output and Comparator output

5. CONCLUSIONS

In present work, An 1-bit sigma-delta analog-to digital converter system has been designed and simulated in standard TSMC 1.8um CMOS Technology. The circuits are simulated in SPICE with MOSIS Level-53 MOS model parameters. For simulation I used Power supply voltage is VDD=1.8v and resistance is 10KΩ and after simulation Gain of Op-Amp is 60dB and Power dissipation s 2.806mW.

6. ACKNOWLEDGMENTS

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