Survey of Multilayer-Graphene Nanoribbons (Ml-Gnr)

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ABSTRACT

Proper interconnect selection has become challenging as technology is shrinking towards dimensions of nanometer. They have a direct impact on power dissipation, time delay, crosstalk and area. As technology is becoming more advanced day by day, need for more reliable interconnects have become very important. From copper to carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), performance based on various parameters is compared. It is clear, multilayer graphene nanotube ribbons (MLGNR) outperform other candidates at various technology nodes. Effect of intercalation doping with different compounds (like pristine, AsF5 and lithium) between the adjacent layers in multilayer GNR has been studied and compared. It has been observed that optimized lithium intercalated MLGNR outperforms the other configurations by giving very low delay and EDP (Energy Delay Product). Also optimization of width plays a great role in reducing noise and crosstalk delay.

Keywords

Interconnects, GNRs, CNTs, Noise, Crosstalk, Performance, Conductivity, Specularity, Current breakdown, Time delay, Power dissipation, Contact resistance, optimization.

1. INTRODUCTION

As we have seen present technology has moved towards dimensions of nanoscale and the operating frequency is in giga hertz. This indicates present systems are having bandwidth in gigahertz, also these complex high performing speedy ICs are at a margin of very low noise as they consume very less power. Therefore, for such IC's, the main cause for crosstalk delay and interference is because of interconnects. The circuit performance of complicated multilayered interconnect system is severely affected by signal coupling and crosstalk delay. Thus VLSI interconnects play a great role in overall system performance. To predict crosstalk for worst case, a crosstalk model which was closed type was introduced for n-coupled lines. This model was entirely RC- based, therefore inductive effects were not considered [1]. Various delay estimation models are presented and showed to be extremely efficient and very accurate. These models have been made enough flexible to be embedded and coded into any design planning or synthesis engine [2]. When chip devices are scaled by a factor of S, there is no effect on resistive potential drop, however inductive potential drop increases by a factor of S. Thus in nanometer technology scaling, proper tradeoff is necessary between resistive and inductive power supply in order to have minimum noise [3]. To maximize the figure-of-merit, a methodology has been introduced for optimizing width of global interconnect. With optimization of wire in nanoscale severe effect on power dissipation, performance and bandwidth is seen [4]. Proper communication throughput can be obtained by introduction of repeaters and scaling of supply voltage. 70% reduction in power dissipation can be obtained with combination of one repeater and 1V supply per millimeter can increase throughput energy to about thrice than that of 2V latency centric interconnect [5]. Various conductance based models are presented, according to these models single layer graphene-nanoribbons below 8nm can perform potentially well than copper lines with unity-aspect-ratio [6]. Parasitic capacitance and capacitance sensitivity is computed using finite-element-method which are based on parameters of nominal geometry and varying geometry parameters respectively [7]. Reducing area doesn't always lead to decrease in power and delay because interconnect capacitance is minimized. A methodology is presented with area as design parameter to decrease power and also reduce thermal runaway [8]. Multi-layer graphene-nanoribbons shows potential to outperform copper below 15nm widths [9]. Properly intercalated with nearly speculated multilayer zigzag graphene nanoribbons have proved better than tungsten (W) and some cases of local interconnects [10]. First time graphene interconnects were integrated with CMOS technology monolithically, graphene interconnects have a frequency around 1.3GHz which is considered high speed in present IC chips [11]. Primary breakdown in graphene happens because of joule heating which is suggested by observing linearly dependent current breakdown on graphene geometry-aspect-ratio. Bilinear graphene shows much better current carrying capability compared to copper, also contact resistance of bilinear graphene and copper is reduced by thermal annealing [12]. Graphene-nanoribbons have shown better performance in comparison to other metallic materials, thus they are considered to be used in 3D ICs. If the length and width of single-layer GNR wire is kept greater, then crosstalk voltage will be higher but not higher than its threshold. While advantages of multi-layer GNR are still superior over copper even in worst case of crosstalk [13]. While increasing Fermi-level time delay is reduced but it increases with increase in interconnect line of transmitted signal [14]. Dynamic delay increases as the length of interconnects keeps on increasing [15]. MLGNR outperformed SLGNR. The overall estimated delay performance is upgraded by 94.5% in case of MLGNR in contrast with SLGNR [16]. RC models was capable of predicting delay but error occurs while estimating frequency response. Thus MTL model is best suited for multilayer GNR to compute their frequency response for large range of frequencies in various RF applications [17]. The resistivity of the zigzag GNR (zz-GNR) have the smaller resistivity than of semiconducting and metallic arm chair GNR (ac-GNR). The resistivity of a mixed MLGNR can be the normal estimation of three kinds of GNRs with various edge geometries [18]. Delay performance is also affected by interlayer distance and doping concentration [19]. Cut-off frequency and delay for wider ML-GNR interconnects with varying edge roughness probabilities are almost constant. Mostly because in wider interconnects, there is

small variation in scattering resistance [20]. Smooth edged MLGNR interconnects exhibit lower crosstalk delay and higher transfer gain in contrast with copper [21].
This paper is organized as follows: Literature survey is given in Section II. Comparison of different parameters is given in table represented by section III. In section IV results and discussions in the form research gaps are presented. Section V concludes the paper.

2. LITERATURE SURVEY

Before the concept of deep submicron, interconnects were not taken into consideration. They were only considered during high precision analysis. As technology keeps on moving down the nanoscale, interconnect selection have become a crucial issue to maintain the signal integrity and overall performance of integrated chips. Copper worked as interconnect for about decade and is still in operation but several other materials are also considered which outperform copper in various ways. One such of a kind is Graphene nanoribbons (GNRs). These are thin graphene strips of width < 50nm, which were first introduced by M. Fujita et al as theoretical model to explore the effect in graphene at nanoscale. Thus single atom size carbon film, which has outstanding properties is regarded as potential replacement for interconnect material. With many miraculous properties of graphene nanoribbons like high current carrying capability, greater current density, high carrier-mobility, extremely great mechanical strength and counting. Graphene has able to break so many standing records because of these properties in case of electricity, heat conduction and strength. The additional thing which makes it more powerful is its atomic thickness, which is around 0.345nm. Based on chirality, graphene nanoribbons can be classified as semiconducting or metallic in nature. These are manufactured according to the requirements. Based on edge structures, graphene nanoribbons are classified as arm chair and zigzag. Armchair GNRs have edges, the segments for each pair is 120/-120deg rotation of previous pair. In case of zigzag GNRs, the edge segment to the previous one is at opposite angle. GNRs can be used as single–layer GNR and Multi-layer GNRs depending upon the requirements. However multilayer GNRs are considered more stable compared to single-layer GNR with varying length of interconnects.

Y. Eo et al [1] have developed a new model for on chip crosstalk delay. As technology started growing faster interconnects became a serious issue in performance analysis for on-chip VLSI circuits. We have seen in past on chip interconnects were not taken into considerations except during high precision analysis. With increase in chip density and decrease in overall feature size, there will be low margin of noise for high performing ICs because of low power and speed. Due complex geometry of interconnects parasitics are introduced which are responsible for power dissipation, crosstalk, signal degradation. Thus affecting the signal integrity of VLSI systems. For CMOS circuits, reliable crosstalk model was given. According to this model, CMOS circuits were change as capacitance at driven port and resistance at driving port. It was observed by implementing this model crosstalk can be predicted easily to maintain signal integrity in high performing ICs [1]. The estimated performance of several interconnect models were presented with analysis of optimized interconnect layout techniques for design planning by J Cong et al [2] These interconnect models are very efficient with high precision makes it worth for high level space exploration devices and design planning for deep sub-micron levels. In comparison with current ongoing complex estimated interconnect algorithms, these models are more accurate and efficient. These models have various applications like during floor-planning these models are used to predict optimized global interconnect behavior, can predict synthesis engine performance, to evaluate various layout optimizations and to optimize delay in various interconnect parameters [2].
As technology is further scaled down, the distribution of power among various networks become very crucial issue in high-performing ICs. The challenging issue in IC design, as current has increased ten times and clock duration is decreased to nanosecond scale, the power supply distribution to retain signal integrity is presented by A. V. Mezhiba et al [3]. The noise due to the power distribution in case of global interconnects is directly affected by the cross sectional scaling of dimensions. This happens because of two things, First: the global layer thickness is not proportionally scaled to minimum line pitch of local interconnect. Second, thickness is scaled proportionally with pitch of local interconnect. It is observed if the metal thickness is kept constant then global line thickness will be constant then the resistive voltage-drop remains constant across power grid however inductive drop is incremented by a factor of S. Also signal-to-noise (SNR) in case of inductive and resistive noise is decreased by s^2 and s respectively. The effect of Inductive noise on on-chip performance is significant as technology is more scaled down as compared to resistive noise [3].
M. L. Mui et al [4]discussed various issues regarding optimization of global lines at nanometer dimensions for VLSI technology are discussed and its impact on bandwidth, power dissipation and overall performance. Wires which are larger in width are proposed in order to reduce resistance per-unit-length (p.u.l) but capacitance p.u.l increases. It has been observed using wide wires adversely degrade performance of chip by increasing delay. An advance methodology was introduced to calculate global line width for given technology, which increases figure of merit (FOM) that is; data transfer rate and delay p.u.l function p.u chip edge. This methodology worked efficiently at 45nm technology node and not at 32 and 22nm nodes. For different FOMs two cases were given for optimum width keep in view line spacing are first: At minimum value keeping space constant, second: keeping both line width and spacing same. These expressions were formed to calculate optimum width of global interconnects. It was observed as line width increases, there is reduction in latency, power dissipation, overall repeater area but it badly degrades bandwidth. Now the relative increment in line width, delay is relatively improved so is repeater area and power dissipation and relatively degraded bandwidth doesn’t pose severe threat to technology scaling [4].
With a focus to decrease power dissipation in global lines analysis of repeater insertion and optimizing voltage scaling is performed [5]. An analytical model was derived to analyze impact of scaling and interconnect length on throughput. It was suggested, there is need to change global wires carrying single binary data to global wires capable of multiple binary bits simultaneously travelling during

latency of line. But this could have severe effect on performance and power of digital circuit by increasing latency and complexity of hardware. However it is mandatory for designers to take into consideration throughput and delay in wire while designing global interconnects for multi-level stack.

To increase the throughput of global wire from single to multi-bit, this was achieved by insertion of repeaters. In fact by the insertion of repeaters, optimization in designs were obtained for different integrated circuits. It has been observed by constant-field-scaling (CFS) throughput is approximately incremented by factor S. in case of global wire scaling, line resistance is 16 times less and is inversely proportional to square of line width. There can be increase in throughput but that requires 4× increment in wire area. In transistor wire scaling depending upon size of drivers, throughput significantly increases with repeaters of optimum size.

With technology scaling down, supply voltage scaling has become necessary and in order to overcome loss due to it repeaters are inserted to maintain the throughput. When supply voltage 2V is scaled to twice of threshold-voltage, there is drop in throughput, thus repeaters should be operated near knee point on throughput curve. Combination of voltage scaling and repeater insertion achieved better throughput 3 times higher than minimum delay point and also decreases power dissipation to about 70% without degradation of throughput [5]. GNRs share properties of carbon nanotubes being a single sheet of graphene. They have similar properties like thermal, mechanical and electronic [6]. Several models were presented which are functions of width, Fermi level, chirality and electron scattering at edges. At 8nm width, GNRs overpower Cu which was observed through these models. Advantage GNR over CNT is more straight-forward fabrication process. In CNTs chirality is random as compared to GNRs. The outcome of GNRs interconnects for previous graphane CMOS nano electronics has been studied. There is zero Fermi energy for ribbon of Undoped graphane (EF=0). It should be metallic or semiconductor that depends on chirality. There is same resistances of semiconductor chilarities and same for metallic to provide large width. Number of MFP and channels of conduction rises due to increment in Fermi level that lowers resistance. The interconnects of nanoscale, there is ultra-small thickness of GNRs that gives better advantage for making capacitances between two interconnects that is 3 to 4 times lesser as compared with 1-2 aspect ratio of copper wires. By stacking graphane layers over all resistance can be decreased. Besides graphane stack sheets to layer after substrate which have non-negative Fermi level and remaining layer are neutral (Ef=0) [6]. The conductance in semiconductor GNR and GNRs wide (>100nm) metallic is same. There is larger resistance in narrow semiconductor GNRs that is less than 5nm widths, hence act as virtually (not-real) insulators. Increase in level of Fermi increases conductance. For 8nm widths and below- the aspect ratio is unity in which GNRs of metallic outperform and wires of copper. Single layer SWCNT interconnect offering small resistance by comparison of GNRs for not really in all width.

H.Qu et al [7] have discussed about process variability becoming critical issue as technology shrinks towards nanoscale, what actually we design and what we finally get on surface of silicon is significantly different. Finite –element-method (FEM) is used to determine capacitive parasitics present in ICs due to capacitive sensitivities and nominal geometry w.r.t geometric parameters subjected to change. This method reduces computation time and errors compared to traditional method. The two main causes of process variation in integrated circuits are First: Chemical Mechanical Process (CMP) which causes thickness variation in dielectrics and conductor thickness. Second: lithography variation which causes change in width and shape of conductor by causing variation in mask, litho focus and energy dose [7]. The best thing about small area of VLSI systems is regarded as suitable for power reduction and delay because of reduced capacitance in interconnects has been presented by J. C. Ku et al [8]. But here it not always favors less area doesn't means less power or delay in nanoscale dimensions, because of thermal effects which sometimes lead to thermal runaway as leakage power which is main source of power dissipation in ICs. Though minimum area enhances yield, but disadvantage is temperature at junction rises also power density increases which exponentially increases subthreshold current. When design area is increased, the in between space of interconnects width and length is increased by same ratio while as width, height and thickness is not changed. Increase in gate size makes it optimum only in case of energy-delay-product (EDP), due to the fact area scaling doesn't change capacitance because coupling and ground components are neutralized. In order to reduce leakage power, thermal model has given at 70nm node with 16 bit adder and technique for area optimization [8].

In case of ML-GNR interconnects, the effect of stacking up various layers of graphene have been studied using current theoretical and experimental values. Comparison of resistance of SWCNT and Copper is done with respect to GNR interconnects shown by T. Ragheb et al [9]. It has been observed ML-GNR outperforms Copper interconnects at width less than 15nm. In the way to model GNR interconnect resistance, first thing is to identify scattering sources that causes impact on charge carrier transport in GNR. Usually static impurity, defects, phonon scattering and edge scattering. 2D graphene consists of impurities that cause scattering of carriers in a long range [9]. Edge scattering is main difference in semiconductor and metallic GNR, as it changes it band structure. Resistance of both changes with width, on increasing width edge scattering fades out and semiconductor and metallic GNR have same characteristics. GNR wires are least affected by temperature which substantially eliminates delay changes due to thermal changes which makes it superior over CNT and Copper interconnects.

The representation of analysis in delay and conductance for GNR interconnects is described by C. Xu et al [10]. GNR model can be derived by deriving three models like conductance model, Tight binding model and the linear response Landauer formula. Conductance of GNR is compared with COPPER, TUNGSTUN, CNTs. To match the outcome of Copper or CNT bundles at global or local level with multiple ZigZag-eddged GNR layers has using doping. Metallic or semiconducting GNR structures can be made on demand because of varying patternability [10]. It has been investigated that GNRs suffer with edge scattering causes remove the impact of MFP, on other hand of CNTs, there are no issue like that. Monolayer type of graphane have better MFP and conduction.

While as, many layer graphane have more less conduction as per layer with effect of intersheet hopping of electron. With having more resistance in one layer of graphane, eventually need of technology for many layers of graphane. In case of many GNRs, conductance and MFP is decrease due to hopping of electron, which is not good to width. Now in-plane conductivity of multiple layer GNR should be obtained by intercalation dope process, there is addition of single dopant layer in between every couple of layers of graphene. With intercalation both current density and MFP can be incremented because scattering due to interlayer is suppressed. Beyond 22nm the better bundles are SWCNT bundles in technology node, rather other GNR structures not good in comparison with local and global wires. It's also predicted that AsF6 doped GNRs have lighter delay in signal as compare with Cu in technology at 11nm node for global lines. If specularity parameter (p) quite near to 1, then AsF6-doping multiple layers zz-GNRs be far better as compared with Cu [10].

First demonstration of graphane interconnects is presented, which is monolithically integrated with 5 stage standard CMOS operation work for this oscillator in operating range more than 1GHz, this is big achievement in electronics. Also first experimental results of performance comparison between MWCNT and graphene on chip interconnects are presented by X. Chen et al [11]. Graphene interconnects working up to frequency of 1.3GHz, this is proportionate with fastest performing speedy processor chips in current scenario. Capacitance related to these interconnects generally the processor consumption of power is subjected to up to 50%. CMOS 5-stage fabrication of ring oscillator by using technology of CMOS in 0.25micrometer. Interconnect in single graphane is integrated with all ring oscillator in order to characterization of all graphane with each single interconnect while oscillation to high speed is maintaining. In order to demonstrate interconnects of graphane has capacity of routing with high speed, the amplitudes and frequencies of ring oscillator by bonding of wires in the previous CMOS chip processed to package of array in pin grid and high frequency testing of electrical the package into a printed circuit board [11].

In this, ring oscillator work in Gigahertz frequency with 80 micrometer long interconnects of graphane which certify the high graphane potential in VLSI interconnects for future vision. Graphene possess low resistivity and can thus offer high frequency. But it's seen with same resistance, MWCNT is able to offer far better delay performance. It may be because wide stripes of graphene have large capacitance. Scaling down graphene width reduces the interconnect capacitance, however it gives rise to issues like increment in contact resistance and wire resistance because edge roughness and material quality should not go beyond limit. Chirality managed graphene ribbons can be possibly created [11]. The key responsible limiting features of two layer graphene and Cu hybrid interconnects are investigated by exploring the behavior which leads to breakdown due to current and BLG and copper contact which is discussed by T. Yu et al [12]. From result it was observed that BLG shows great current density (~100 times > Cu), and contact resistance of BLG/Cu can be significantly reduced by dc current-induced thermic annealing. Thermal annealing as reported helps in upgrading conduction in the graphene, as it possibly lowers contact resistance. Although thermal annealing mostly introduces contamination if graphene gets exposed to the air. Before annealing, the estimated BLG to Cu contact resistance is nearly infinite. For voltage sweep from 0 to 1v resistance is still in order of giga ohms. For voltage sweep from 0 to 3v samples exhibit linear I-V characteristics. For low bias voltage 5mV, the resistance is found to be on order of kilo ohms [12].

Electrical measurement depending on time were performed to examine electrical stability of BLG or Cu contact, even after high bias voltage pulses, its seen contact resistance remains same ~12kohm. However, there is increase in resistance almost thrice from 12 to 35kΩ if exposed to air for about two and a half hour. The current-breakdown of BLG occurs at about 4mA. If BLG with 4 micrometer line width and of 0.7 nm flake thickness (0.35nm for MLG), then at breakdown the average current density is about 3 × 〖10〗^8 A/cm^2, to the comparison of CNT and GNR breakdown induced current density. It has been observed that breakdown current is proportionate to aspect ratio, showing joule heating techniques. Similar linear correlation is observed in BLG, TLG and MLG between breakdown and aspect ratio. TLG exhibits improved breakdown characteristics [12]. Breakdown is caused due to damage near the contact and these failure sites are located always at metal fingers, which causes voids in copper. So it has been clear copper diffuses into graphene and local copper depletion leads to cracks and failure of the copper contact. In order to check the reliability of GNRs for 3D designing of ICs, signal integrity is analyzed for Single layer GNR and Multilayer GNR interconnects based on ESC models, crosstalk impact on both is theoretically characterized. Although it was observed that SLGNR results in larger crosstalk delay due to large interconnect width and longer length. In case of multilayer GNR though it has worst crosstalk but it is still preferred due to its advantages over copper [13]. If threshold voltage is assumed to be 0.25V, there will be seen no logic error due to crosstalk produced in SLGNR, even at 1000 micrometer interconnect length for tri SLGNR. Therefore considered better reliable in comparison to Aluminium and copper also to single walled CNTs. With the help of coupling capacitance, crosstalk can be determined, further if proper spacing is used among the all SLGNRs. ML-GNR at intermediate level possess a time delay which is function of length of GNR can be estimated. Gate size is kept larger 50 times than load and driver for intermediate interconnect. The results show that full specularity possessing ML-GNRs can outperform copper. MLGNR possess low peak voltage compared to copper, thus has advantage and can be used high technology nodes [13]. Various characteristics of signal transmission were obtained for multilayer GNR using ESC model and comparing their transient responses with this model while considering both inductive as well as capacitive coupling that's is present in GNRs adjacent layers. Transfer function is derived to predict output waveforms for voltage by analyzing 4th order approximation at 14nm and 22nm technology [14]. It was observed that while increasing Fermi level, there is reduction in time delay. However, it increase with increase in interconnect line of transmitted signal. The ML-GNR interconnect inductance p.u.l and resistance p.u.l depends on Fermi level, which makes crosstalk sensitive to variation.

ML-GNR interconnects have shown various superior features over copper and other carbon components presented by N. Reddy et al [15]. Thus delay is very crucial parameter which needed to be optimized. The out phase delay and in phase plays great role, by using a

bus architecture with 2-coupled wire implementing CMOS driver circuit can be analyzed. By using different layer number like 4 to 10 finally 20, the impact of dynamic crosstalk is analyzed in multilayer GNR. From the results it was clear that dynamic delay increases as length on interconnects goes on increasing, also impact of out-phase is higher and there is more increment in out-phase in comparison to in-phase. Two case are given, first: transition of both lines in similar direction that is in-phase second; transition in opposite direction that is out-phase. The Miller-Coupling-Factor (MCF) is used to estimate dynamic crosstalk, for in-phase MCF=0 and for out-phase MCF=2. Thus out-phase can be termed as worst case for global lines. Although dynamic delay has been improved with higher number of layers by 18.04% for out-phase and 4.75% for in-phase. It makes ML-GNR potentially better to be used at global length [15].

MLGNR outperformed SLGNR. The overall estimated delay performance is upgraded by 94.5% in case of MLGNR in contrast with SLGNR. GNRs are unrolled version of SWCNT therefore they have almost similar electronic properties demonstated by M. K Majumder et al [16]. Graphene can be classified depending upon its chirality into armchair GNR and zigzag GNR (ac- and zz-GNRs respectively). Band structure of GNRs is calculated using tight binding model. The arm chair GNRs are divided in metallic arm chair and semiconducting arm chair GNR given on number of hexagonal rings (N) present over width of GNR which are length fixed. To be metallic in nature N=3p-1 and 3p+2 for semiconductor N=3p and 3p+1. Zz-GNR for sure are metallic and independent of N. Equivalent contact resistance (Rc) depends on fabrication techniques in case of ML-GNR interconnects. From current fabrication technology, GNR exhibits an imperfect contact resistance of 3.2kΩ at both ends of interconnect line. The equivalent RLC model for MLGNR takes into account scattering effect and conductance modeling of GNR. The reason behind using conductance modeling in case of ML-GNR is to obtain scattering resistance of ML-GNR. Scattering mostly occurs because of defects, roughness on line edge which leads to scattering, static impurity and acoustic phonon scattering [16]. λL represents MFP of carriers when is impurities are present. The quantitative value of λL is taken as 0.42µm and 4µm for MLGNR and SLGNR respectively. Using a DI L system employed by CMOS driver is utilized to estimate delay for SLGNR and MLGNR. For both SLGNR and MLGNR equivalent RLC model is used as interconnect wire in Driver Interconnect load and interconnect wire is ceased with load capacitance CL = 10AF. For both Single and multilayer GNRs, HSPICE simulation were performed for different layers like 4, 10 and 20. It is observed for lengthy interconnects, delay increases whereas goes down with increment in number of GNR layers and width. Conducting channel are increased in number with increased width of GNR, which results in lesser propagation delay. A reduction in resistive parasitics is seen on increasing number of layers. MLGNR with Nlayer = 20 results in lower effect of delay in contrast to Single and Multilayer GNR with Nlayer = 4 or10. Hence Multilayer GNR is more efficient with increased number in layers for global wires [16].

Several models have been derived for different types of interconnects so far. It has been seen in order to estimate delay RC distributed models show 15% less error as compared to other. Multiconductor-transmission-line (MTL) models are used in case of RF design circuits because here frequency response should be more accurate. RC models are used to estimate energy delay-product and crosstalk for future technologies. While comparing the performance of models, it was clear RC models was capable of predicting delay but error occurs while estimating frequency response. Thus MTL model is best suited for multilayer GNR to compute their frequency response for large range of frequencies in various RF applications. However RC model is enough ML-GNR to be modelled in digital circuits [17].

Equivalent single conductor (ESC) model is the basic to have information about transmission characteristics and the distributed parameters of MLGNR. The relation between number of conducting channels with width and Fermi level is proportionate. It can be taken from the ESC model that MLGNR can be considered as stacked SLGNRs, because they have do not affect each other. Total layer number is determined by n = 1+Inter (H/ δ), where "Inter(・)" denotes that only the integer part is considered. Between the adjacent layers the interval spacing is δ = 0.34 nm, which is the Van der Waal's gap [18]. The resistivity of the zigzag GNR (zz-GNR) have the smaller resistivity than of semiconducting and metallic arm chair GNR (ac-GNR). The resistivity of a mixed MLGNR can be the normal estimation of three kinds of GNRs with various edge geometries. To assess their definitive potential for the interconnect design, it is expected that MLGNRs just comprises of metallic ac-GNRs with the equivalent width W, Fermi vitality EF, and specular constant p. Resistivity is same for the semiconducting ac-GNRs and metallic ones and left no reason to have the effects of semiconducting ac-GNRs on regular performance or in other words advantage over the SWCNT bundle. The quantum contact resistance Rq (= 12.9/Nch kΩ) of SLGNR can be obtained by the number of conducting channels Nch , which is a function of W and EF. The Fermi energy of MLGNR ought to be enhanced by adopting a proper doping strategy to stifle its ban87 and screening effects, while the interval spacing between adjoining layers can be kept [18]. Fermi energy is much proportional to the conducting channels, as fermi level rises conducting channel value also become higher. Fermi level having value higher than 0.1 eV, may led to disregarded fabrication accuracy. Because of the large width of the GNR the adjacent layers in MLGNR behaves as parallel plates. Then the values of the per-unit-length (p.u.l)coupling inductance and capacitance is given by

$l_m = \mu_0\delta/W$, and $c_m = \varepsilon_0 W/\delta$.

MLGNR interconnect geometry and encompassing dielectrics are used to control the p.u.l. magnetic inductance and electrostatic capacitance in the ESC. This is much possible in recent technologies. Layer numbers in the ESC models of the MLGNR interconnect have the elements as per unit length, equivalent inductance and capacitance. The equivalent inductance diminishes as the layer number increments, while the equivalent capacitance rises at first and after that leads to a particular value when the layer number value is higher than 5. To justify the statements , and comparing the outcomes to the MWCNT the equivalent inductance of the MWCNT

diminishes with the shell number.. However, for shell number larger than 5,equivalent capacitance value increments linearly. The reason holds is, for each layer of the shell in MLGNR in every case kinetic inductance is substantially larger than the magnetic .Hence, the kinetic inductance has predominant impact in the ESC models of both MLGNR and MWCNT. A suitable technique can be considered as the phonon coupling from the dielectric can thereby be ignored in the MLGNR. Thus, deformities and edge scatterings are used to have the approximation of effective MFP. For a suspended graphene value of MFP corresponding to the scattering by defect d is approx to 1 μm . But intersheet hopping led to decrease in the value to 419 nm [18]. The usage of carbon nonmaterial as a interconnect is neutralized by the presence of larger device resistance. It may be very well taken in consideration that at this point execution of MLGNR and CNT are nearly equivalent to that of Cu wires. Presently, our consideration is centered around the MLGNR interconnect at the global and intermediate levels. The sizes of load and driver are around 100 and 50 times greater than the required gate size for global and intermediate levels, respectively. The MLGNRs with completely specular edges appear better in performance over Cu wires, and this quality can be exploited in future technology nodes. However, the benefit of MLGNR interconnects tends to reduce from global to intermediate level, which is actually because of the dissimilarity of resistivity if Cu at various levels. Also, there is much proportionate of Cu wires at intermediate and global level for the value of p=0.8 .As the technology is scaled down, at the intermediate level in MLGNR a smaller delay is noticed. The operation of MLGNR interconnect is inferior to its Cu counterpart for a interconnect of length 10 μm . The time delay ratio rises gradually with the further increase in length. The benefit of MLGNR interconnect with top contacts will be augmented with the technology progressed. All things considered, the side contacts can give littler resistance than the top ones for the short interconnect. Nonetheless, as the length expands, between the adjacent layers the perpendicular resistance in the MLGNR decreases, which makes their resistance and operation with various contacts end up shut. The crosstalk in the MLGNR interconnects at intermediate level is portrayed, in specific for cutting edge technology node, and the benefits of MLGNR interconnects over Cu wires won't be debased by the crosstalk impacts [18].

It has been observed variation in line resistance has a great impact on dynamic crosstalk and noise in case of ML-GNR. Doped multilayer-GNRs with perfect specularity are found to have great tolerance against variations in line resistance independent of technology. It was clear percentage of variation in the line resistance is similar to percentage of the signal transmission, whereas percentage of noise voltage changes with percentage of line resistance. Its well-known fact variation in various parameters have impact on performance of ML-GNR like interconnect width shown by M. Sahoo et al [19]. MFP, dielectric thickness and constant. Delay performance is also affected by interlayer distance and doping concentration. ML-GNRs have conceivably provided appealing answers in a seriously developing research zone of interconnects. Also for MLGNR interconnects, doping is inescapable because the conductivity of neutral MLGNR couldn't even reach to Cu. In this way, doped MLGNR may possibly display vey less resistance in contrast with Cu wires [20]. Delay, bandwidth and power performances of Cu and doped MLGNR are compared using Equivalent single conductor (ESC) model. It has been seen the overall power dissipation and delay in doped MLGNR is significantly reduced by 43.72% and 86.13% respectively, in contrast with the Cu interconnects.

In order to analyze RLC circuit model it requires very computational effort, therefore accurate and but simplified equivalent single conductor (ESC) model is utilized by consolidating a blemished MLGNR contact resistance and realistic parasitics of driver. A transfer function is derived, utilizing a driver-interconnect-load (DIL) system and is utilized to find Nyquist stability and bandwidth, at global interconnect, intermediate and local lines for MLGNR (doped and neutral) and Cu. The contact resistance (Rmc) of imperfect metal-MLGNR has particular value starting from 1 kΩ to 20 kΩ. Each layer of MLGNR shows lumped quantum resistance (Rq) that is because of the quantum incarceration of carriers over the interconnect width. Each layer in MLGNR involves quantum capacitance and kinetic inductance that shows the density of electronic states and mobile charge carrier inertia respectively. The electrostatic capacitance is because of the field coupling between the ground and bottom layer. Along these lines, electrostatic capacitance is basically depends on MLGNR distance (d) and width (w) from ground plan. Also the inductance of MLGNR is because of stored energies in the magnetic field due to carriers. Power dissipation and propagation delay are proportional to the capacitive and resistive parasitics of interconnects [20]. Thicker doped MLGNR shows considerable decrease in power dissipation and crosstalk delay when contrasted with copper interconnects. The doped MLGNR shows higher carrier concentration in all layers which significantly increments number of conducting channels which in turn radically lessens resistive parasitic contrasted with Cu interconnects. Although, quantum capacitance is increased due to the increase in conducting channels number in the doped MLGNR however the equivalent capacitance remains relatively steady. Consequently, the total impact of resistive parasitic and equivalent capacitance of doped ML-GNR decreases the total delay also the power dissipation in contrast with copper interconnects. Independent of ML-GNR and Cu, the cut-off frequency decreases for lengthy interconnects. The essential purpose for this decrease is higher resistive parasitic and equivalent capacitance that mainly relies upon the interconnect lengths. Also, variation in cut-off frequency given for Cu and doped ML-GNR is greater at semi-global (l= 500μm) and for global (l = 2500μm) lines contrasted with the local (l = 5μm) interconnect length. In this manner, doped MLGNR shows an enhanced 3dB bandwidth contrasted with copper at intermediate and global interconnect lines. For doped MLGNR the bandwidth is independent of width. The intercalation doping in MLGNR between the surrounding layers increases the mean free path (MFP) of electrons. The Higher MFP and number of layers decreases the resistive parasitics with a very small increment in equivalent capacitance, which results in enhanced bandwidth as compared to Cu interconnects [20]. The viable MFP in case of GNR is reduced due to the presence of edge roughness. Because rough edges lead to the scattering of electrons at edges, which makes MFP width dependent. The MFP correlating with diffusive scattering produced at edges, taken as function of the edge back scattering probability (P) and also average distance that an electron covers before hitting the edge. It has been seen the cut-off frequency and delay for wider ML-GNR interconnects with varying edge roughness probabilities are almost

constant. Mostly because in wider interconnects, there is small variation in scattering resistance. In case of narrow width MLGNR, system has attained more stability (for P = 0.1), because of the higher scattering resistance. On the other hand, for the wider interconnects, change in stability is ostensible for various scattering probabilities at edges. A noteworthy change is seen in performance for the narrow-width ML-GNR with greatest edge roughness probabilities [20].

For a pair of coupled MLGNR interconnect, a distributed circuit model is given, with both inductive and capacitive coupling is taken into consideration. Smooth edged MLGNR interconnects exhibit lower crosstalk delay and higher transfer gain in contrast with copper. However because of present fabrication process edge roughness is mostly inevitable that remarkably deteriorates the overall propagation performances. In case of wider MLGNR interconnects the performance variation due the edge roughness is slightly less. Besides it the demonstration that side-contact MLGNR lines have preferred electrical performance over top-contact ML-GNR lines taken at short line length in contrast with longer interconnects due to control resistance in every layer [21]. The in-phase transfer gain at the 100MHz and at 1GHz operating frequency of 1000µm line attains 0.94 and 0.25, respectively, while out-phase transfer values are 0.47 and 0.018. This is because in out phase case the values of coupling capacitance gets doubled, which in turn decreases transfer gain although there is increase in decoupled equivalent capacitance. As wire-length is linearly proportional to interconnect equivalent parasitics, there is increase in crosstalk delay with wire length. Also crosstalk delay is greater at out phase than at in-phase case because of Miller effect. The crosstalk delay values at in-phase case for 100µm and 1000µm are only 41.8ps and 669.8ps respectively, whereas crosstalk delay values at out-phase case are 74.8ps and 3.54ns. In order to reduce power dissipation, IR drop and propagation delay and thereby decrease wire resistance, the width of global line is generally much greater in width as predicted by ITRS. In case of narrow width ML-GNRs the presence of the rough edges that remarkably causes reduction in mean free path of the electron and also raises the wire resistance. With increasing wire width it has been observed that the transfer gain also increases. This happens because the increment in the wire width causes increment in the No. of conducting channels and also decreases the resistance of wire remarkably. Thus the transfer gain of MLGNR interconnects in comparison with copper is small [21]. Also the transfer-gain of ML-GNR interconnects increases with increment in Fermi-level. This is because the high Fermi level causes reduction in the wire resistance and enhances the interconnect transfer-gain. The difference in transfer-gain for top-contact ML-GNR and side-contact ML-GNR is greater at the short wire length (lGNR=100um) in contrast to the short wire length (lGNR=1000um). It happens because value of the inter-layer resistance is very less as compared to in-layer resistance at longer wires. ML-GNR interconnects not always have the better propagation characteristics than copper. MLGNR interconnects would have high crosstalk delay due to high edge scattering probability. The fact is mean free path is reduced by edge roughness, thereby, increases the crosstalk delay and equivalent interconnect resistance [21].

The reliability of copper wires due to various parameters like power dissipation, latency and dynamic crosstalk degrades significantly in nanoscale regime presented by M. G. kumar et al [22]. This happens because of the scaling down of electronic devices to many fold improvement of interconnect lines in VLSI technology. On the other hand, CNTs because of their particular properties like current density, mechanical strength and high thermal conductivity have been taken into consideration to be used as interconnect material. Various CNT configurations such as mixed-wall CNT bundle (MCB), multiwall-CNT (MW-CNT) and single wall-CNT (SW-CNT). The performance of the CNT interconnects is estimated using driver-interconnect-load system. In case of MCB interconnect, propagation delay is reduced by 22%, 40%, 60% and 69% in comparison with MWCNT bundle, MW-CNT, SW-CNT bundle and Cu interconnects respectively. This analysis takes into account 32nm technology node with interconnect length difference from 500 to 2500 micrometer [22]. In MCB interconnect the reduction in power dissipation for same dimension is 36%, 45%, 49% and 60% in comparison with MWCNT bundle, MWCNT, SWCNT bundle and copper interconnect respectively. CNT are actually structures which are obtained from graphene sheets. A CNT is also defined as rolled-up sheet of graphene, edges of which are tied together to make a seamless cylinder. Its clear zigzag-CNTs (zz-CNT) have the chiral index of which the n1 or n2 = 0, on the other hand the arm chair (ac-CNT) have index of which n1 = n2. SWCNT can be either semiconducting or metallic depending upon the direction in which the sheet is rolled. The physical model of SWCNT interconnect is similar to that of copper interconnects. The CNT resistance can be given as a function of length of electron MPF (lmfp) and interconnect length (l) it's observed resistance can exhibit either linear relationship or exponential relationship. Thus, SWCNTs are quicker than Cu wires, if MFP of electron is around 1-10 micrometer. The general performance of SWCNT is bounded. This happens because of high values of kinetic inductance and resistance which results in higher latency and lower conductivity. These reduces the system performance. A possible way to overpower this problem is to use SW-CNT bundle [22].

As isolated SWCNT can't fulfill the performance criteria, a SW-CNT bundle structure often used for interconnect purposes. The values of kinetic inductance and resistance are reduced in case of SWCNT bundle. In case of SWCNT, just one third of SW-CNTs is metallic, rest two third behaves like semiconductor, this happens due to disparity in chiralities and limitations in fabrication of SWCNTs bundle interconnect. The overall number of the SW-CNTs in a bundle (NSWCNT) plays an important role while calculating parasitic values of wires. It significantly improves conductivity and latency of wire by reducing kinetic inductance and quantum resistance. Its seen that resistance of SWCNT is less in contrast to copper wires. SW-CNT interconnects out-perform copper in case of resistance, as SWCNTs have less resistance than copper interconnects. By enhancing the SWCNT diameter, more space between adjacent lines and by reducing line length. SWCNT bundle reduces power dissipation up to four orders of magnitude in contrast with

copper interconnect. However SWCNT bundle performance is limited by CNTs metallic density and faulty contact resistance. The skin effect in case of CNT bundle interconnects is comparably less as comparison to Cu wires, mostly due to greater kinetic inductance in CNT bundle interconnect. Various layers of concentric shell like structure with different diameters form MWCNT. The fabrication process of MWCNT is easier as compared to SWCNT because growth process is under control. MWCNTs are considered reliable for interconnect applications due to better electrical conductivity, irrespective of diameter of layers. There is no restriction whether layers are semiconducting or metallic. The propagation delay for both SWCNT and MWCNT is proportional to interconnect length, but its gets reduced with increased number of SWCNTs in bundle and increase in shell number [22]. The applications of MWCNT is seen in case of global interconnects, as they are mostly metallic and carry low resistivity compared with SWCNT bundle. In comparison to copper and bundle of SWCNT, it provides better signal integrity at global level. MWCNT doesn't suit at local interconnects because of higher delay. MWCNT bundle consists of both SWCNTs and MWCNT and performs outstanding than SWCNT and MWCNT alone at global level. However MCB outperforms all structures of CNT as well as copper, providing reduction in propagation delay, crosstalk and power dissipation. Thus making MCB more efficient and best options for VLSI interconnects in future. Interconnects which are supposed to sustain high temperature should also support low temperature (600K to 50K respectively). Variation in temperature can greatly have impact on parameters like length, width etc. GNRs outperform copper at various temperatures [23]. In multi-layer graphene nanoribbons, doping of lithium is done between the adjacent layers to obtain better performance in comparison to copper interconnect. Li-intercalated multi-layer graphene nanoribbons is considered for local interconnects. At local interconnects it has become great issue that interconnect delay overpower the transistor delay [24]. Before Lithium, Asf5 was used for intercalation. The thickness of both Lithium and ASF5 doped interconnects were optimized to give lowest energy delay product (EDP) and delay. Even if in case edge roughness is considered, optimized TC-MLGNR Li doped is regarded as fastest interconnect and shows very less delay and EDP, irrespective of local interconnect length among all other configurations. It has been, there is reduction in resistance with the increment in thickness of TC MLGNR interconnects. So there is a point where thickness has been optimized due to which, there is minimum value of energy value product and delay. In order to have minimum delay the needed optimum thickness in case of pristine, Li and ASF5 intercalated TC MLGNR interconnect is given as 2.04 nm, 1.85 nm and 2.875 nm with smooth edges respectively while with rough edges(p = 0.2) is 4.08 nm, 4.81 nm and 5.75 nm at gate pitch length of 100. Also when these optimal thickness are compared they show less capacitance in contrast with copper [24]. Now far we have seen MLGNRs have been doped with pristine, ASF5 and Lithium. Here with a combination of better quality multi-layer graphene nanoribbons with layer count under control, intercalation with FeCl3 and optimized design for GNR, it is possible to have much great performance and better reliability in contrast to copper at the stretch of 20 nm width is presented by J. Jiang et al [25]. Its investigated that up to this work there is experimental record on intercalated GNRs that indicates both improved electrical conductivity and reliability enhancement so that it concludes GNRs as future interconnect material. In this context 100 above MLGNRs were fabricated using interconnect design, and then simulated and optimized. Its observed that intercalated MLGNR interconnect exhibit analogues resistivity and approximately better performance than copper. The extremely important feature that is tremendously high current carrying capacity makes it superior over conventionally designed interconnect approaches [25]. During intercalation process its observed that there is increment in roughness of surface of SiO2 substrate and Line-Edge-Roughness (LER) of MLGNR interconnect by FeCl3 doping. The estimated standard deviation of LER is ~4 nm and ~2.5 nm for doped and undoped GNR respectively. It has been observed that doping time effects resistivity. If doping is performed for 10 hour period then carrier concentration on surface increased to 1.75×1014 cm-2 (doped) from 3.88×1013 cm-2 (undoped). Although 10 hour intercalated MLGNRs show reduced resistivity than 5 hour intercalated MLGNRs. Nevertheless by increased doping period the electrical conductivity of GNR is enhanced potentially but allowing it beyond a limited level can degrade over all GNRs conductivity by additional surface roughness and scattering. The noteworthy reliance of doping degree on MLGNR has been identified, which show that for 20nm width, electrical conductivity of GNR is enhanced further to overpower copper at same dimensions. Thus MLGNRs interconnects with increased reliability and optimized process, they pave feasible way for future ICs and interconnect technology based on carbon [25].

As it has been seen by increasing width (w) and length (l) of interconnects, there is increment in relative stability for TC-GNR, SC-GNR and copper interconnects. Also copper interconnect outperforms SC-GNR and TC-GNR in stability analysis because of high phase and gain margin for interconnect length ranging from (10-100micrometer) [26]. Although copper and TC-GNR have relatively similar stability. But there are several other benefits of TC-GNR which makes it superior than copper and SC-GNR interconnects to be used at various technology nodes. TC-GNR has advantage over SC-GNR, its fabrication process is easy compared to later one which makes it more preferable than SC-GNR. On the other hand, SC-GNR is better in terms of electrical circuit view point. It's more preferable, because overall resistance is reduced as compared to TC-GNR. Using phase margin (PM) and gain margin (GM) bode stability can be measured. For a system if gain and phase margin is increased then stability will increase. Analysis for bode stability is performed at various technology nodes like 11nm, 16nm and 22nm for interconnect length (10-100nm). Its seen with increment in length, the gain and phase margin increases which in turn increases relative stability [26].
The value of both gain margin and phase margin is greater for copper at 100 nm interconnect length ~120 dB and ~150 (in degree) respectively. For TC-GNR the values are ~118 dB and ~148 (in degree), for SC-GNR ~82 dB and ~142 (in degree) respectively. Though copper and TC-GNR have almost similar stability but there are other reasons like electromigration and scattering effect where TC-GNR dominates and is considered more reliable. Analysis for bode stability for varying interconnect width is also performed. Its

observed with increment in width there is increase in relative stability. TC-GNR outperforms both SC-GNR and copper in stability and is considered more viable. Thus can be used in VLSI chip design as nano interconnect [26].

Multiwalled Carbon Nanotube (MW-CNT) interconnects is an efficient interconnect design with high current density and is considered best possible solution for next generation on chip interconnect [27]. It is seen that out phase and in phase delays for Cu interconnect is closely around 2.7× and 2.5× times greater than MW-CNT interconnects. In both techniques USFDTD (Unconditionally Stable Finite Difference Time Domain) and FDTD (Finite Difference Time Domain), the average error incorporated w.r.t. HSPICE is 0.82% and 1.1% respectively. Also for 1000micrometer interconnect length peak-noise voltage is 6% greater in Cu as compared to MW-CNT interconnect. It can thus be concluded that very small latency is associated with MW-CNT interconnects. Analysis of current density of MW-CNT and Cu is observed as 6×〖10〗^13 A/m^2 and 4×〖10〗^13 A/m^2 respectively. So MW-CNT have current density 1.5 times greater than copper. Also copper reliability is degraded because of surface scattering and electromigration, on the other hand MW-CNT shows great stress resistance capability, thus beating copper in future interconnect race [27].

As technology is becoming denser day by day, both interconnects and devices are facing challenges due to variation in temperature and power dissipation have become more critical. As we know power dissipation is inversely related delay, the fact is if delay is somehow reduced the power dissipation will also be reduced to great extent [28].

Analysis for power dissipation is conducted with varying layer number. MLGNR with 11 layers, low resistance and capacitance is seen. But talking about time delay and power dissipation it gets better with 15 layers. Thus MLGNR with 15 layers are suitable interconnects.

Width of ML-GNR has been optimized by reducing noise parameters like noise area, noise peak, noise delay and crosstalk interference for global as well as intermediate interconnects by using ABCD parameter model at 11nm technology node [29]. Analysis of crosstalk noise is performed for copper and ML-GNR interconnects, its observed for ML-GNR intermediate interconnects with width 10nm above and global length from 50 to 100nm, the worst case delay with perfectly specular (p = 1) is less in comparison to copper. Talking about noise immunity, perfectly specular ML-GNRs has comparably better immunity than copper. In order to make ML-GNRs to perform extremely well, width is optimized for intermediate interconnects in a range 10 to 20nm and for global interconnects in a range 50 to 100nm. Its investigated nearly and perfectly (p = 0.8 & 1 respectively) ML-GNR interconnects are most reliable and promising for future on chip VLSI interconnects. In case of Horizontal Multilayer Graphene Nanoribbons (HGNRs) the problems arose because of electrical contact, these challenges were solved by Vertical Graphene nanoribbons (VGNRs) [30]. Moreover, comparatively all the labor to date has been given to carbon nanotubes (CNT) and Horizontal GNR. It is also observed that CNT and HGNR maintain better performance and are more reliable in contrast with copper. But thermal problems of HGNRs was a critical issue which was overcomed by VGNR. More important thing about VGNR is that unlike HGNR, electrical conductivity is very high in VGNR due the fact that every layer participate in electron transport. As technology keeps on moving down, resistivity is kept unchanged of perfect specular GNRs, irrespective of horizontal or vertical forms. Also for such GNRs effective resistance doesn't dependent on orientation and size. It is observed for nearly specular (p = 0.8) vertical GNR and horizontal GNR shows smaller and larger resistivity in contrast with copper. VGNR is still more advantageous over HGNR, though difference reduces slowly with increment in Fermi energy and specular parameters. This difference can however be removed by increasing specularity parameter (p). VGNR still holds lead in case of delay over HGNR and copper [30].

3. OBSERVATION TABLE

S.No	Authors/Year	Publisher	Title	Parameters	Observations
1	Y. Eo, W. R. Eisenstadt, J. Y. Jeong, O. K. Kwon / 2000	IEEE Trans.	A New On-Chip Interconnect Crosstalk Model and Experimental Verification for CMOS VLSI Circuit Design	Crosstalk, effective capacitance and resistance, distributed model	A closed crosstalk model was developed for multiple lines. This model could easily predict the crosstalk to maintain the signal integrity for high performing circuit designs.
2	J. Cong, Z. Pan / 2001	IEEE Trans.	Interconnect Performance Estimation Models for Design Planning	Driver sizing, wire sizing, buffer insertion and sizing, design planning, interconnect estimation	Several interconnect optimization models are introduced. These delay estimation models are flexible enough to be coded and embedded into any design planning or synthesis engine.

3	A. V. Mezhiba and E. G. Friedman / 2004	IEEE Trans.	Scaling trends of on chip power distribution noise	Power supply noise, Power distribution technology Scaling	The challenging issue in IC design, as current has increased ten times and clock duration is decreased to nanosecond scale, the power supply distribution to retain signal integrity
4	M. L. Mui, K. Banerjee and A. Mehrotra /2004	IEEE Trans.	A Global Interconnect Optimization Scheme for Nanometer Scale VLSI With Implications for Latency, Bandwidth, and Power Dissipation	Bandwidth, global interconnect optimization, critical inductance, interconnect power Dissipation optimization, , delay per unit length,	An advance methodology was introduced to calculate global line width for given technology, which increases figure of merit (FOM) that is; data transfer rate and delay p.u.l function p.u chip edge.
5	V. V. Deodhar and J. A. Davis 2005	IEEE Trans.	Optimization of throughput performance for low-power VLSI interconnects	High throughput, low power, interconnect performance, , wave pipelining, repeater insertion	To increase the throughput of global wire from single to multi-bit, this was achieved by insertion of repeaters. In fact by the insertion of repeaters, optimization in designs were obtained for different integrated circuits.
6	A.Naeemi, James D. Meindl / 2007	IEEE	Conductance Modeling for Graphene Nanoribbon Interconnects	chirality, width, Fermi level	The conductance in semiconductor GNR and GNRs wide (>100nm) metallic is same. Increase in level of Fermi increases conductance. For 8nm widths and below- the aspect ratio is unity in which GNRs of metallic outperform and wires of copper. Single layer SWCNT interconnect offering small resistance by comparison of GNRs for not really in all width.
7	H. Qu, L. Kong, Y. Xu, X. Xu and Z. Ren /2008	IEEE Trans.	Finite-element computation of sensitivities of interconnect parasitic capacitances to the process variation in VLSI	IC parasitic extraction, Jacobian derivative, sensitivity analysis process variation.	The two main causes of process variation in integrated circuits are First: Chemical Mechanical Process (CMP) which causes thickness variation in dielectrics and conductor thickness. Second: lithography variation which causes change in width and shape of conductor by causing variation in mask, litho focus and energy dose.
8	J. C. Ku and Y. Ismail /2008	IEEE Trans.	Area optimization for leakage reduction and thermal stability in Nanometer-scale technologies	Layout, leakage, temperature	When design area is increased, the in between space of interconnects width and length is increased by same ratio while as width, height and thickness is not changed.

9	T. Ragheb and Y. Massoud /2008	IEEE/ACM International Conference	On the Modeling of Resistance in Graphene Nanoribbon (GNR) for Future Interconnect Applications	Resistance, Width	It has been observed ML-GNR outperforms Copper interconnects at width less than 15nm. In the way to model GNR interconnect resistance, first thing is to identify scattering sources that causes impact on charge carrier transport in GNR
10	C. Xu, H.Li, K.Banerjee / 2009	IEEE Trans.	Modeling, Analysis, and Design of Graphene Nanoribbon Interconnects	Bandgap, Fermi level, , mean free path and edge specularity	If specularity parameter (p) quite near to 1, then AsF6-doping multiple layers zz-GNRs be far better as compared with Cu
11	X. Chen, D. Akinwande, K J. Lee, G F. Close, S. Yasuda, B C. Paul, S. Fujita, J. Kong, H S. Philip Wong / 2010	IEEE Trans.	Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed CMOS Electronics	Performance and Optimization, speed	First demonstration of graphene interconnects is presented, which is monolithically integrated with 5 stage standard CMOS operation work for this oscillator in operating range more than 1GHz, this is big achievement in electronics.
12	T. Yu, E K. Lee, B. Briggs, B.Nagabhirava, B. Yu / 2011	IEEE Trans.	Bilayer Graphene/Copper Hybrid On-Chip Interconnect: A Reliability Study	Current Density, Breakdown	From result it was observed that BLG shows great current density (~100 times > Cu), and contact resistance of BLG/Cu can be significantly reduced by dc current-induced thermic annealing. Thermal annealing as reported helps in upgrading conduction in the graphene, as it possibly lowers contact resistance
13	W. S. Zhao and W. Y. Yin /2012	IEEE	Signal Integrity Analysis of Graphene Nano-Ribbon	Length, width, crosstalk	Although it was observed that SLGNR results in larger crosstalk delay due to large interconnect width and longer length. In case of multilayer GNR though it has worst crosstalk but it is still preferred due to its advantages over copper.
14	J. P. Cui, W. S. Zhao, W.Y. Yin and J. Hu / 2012	IEEE Trans.	Signal Transmission Analysis of Multilayer Graphene Nano-Ribbon (MLGNR) Interconnects	Crosstalk, inductive and capacitive couplings, time delay.	It was observed that while increasing Fermi level, there is reduction in time delay. However, it increase with increase in interconnect line of transmitted signal.
15	N. Reddy. K, M. K. Majumder, B. K. Kaushik, S. K. Manhas and B. Anand /2012	Computers and Devices for Communication (CODEC), 5th International Conference	Dynamic crosstalk effect in multi-layer graphene nanoribbon interconnects	In-phase and out-phase delay, GNR, MLGNR	From the results it was clear that dynamic delay increases as length on interconnects goes on increasing, also impact of out-phase is higher and there is more increment in out-phase in comparison to in-phase.

16	M K. Majumder, K. N. Reddy, B K. Kaushik, S K. Manhas / 2012	Computers and Devices for Communication (CODEC), 5th International Conference	Comparison of Propagation Delay in Single- and Multi-layer Graphene Nanoribbon Interconnects	Propagation delay	The overall estimated delay performance is upgraded by 94.5% in case of MLGNR in contrast with SLGNR. Thus MLGNR can be considered future candidate for IC designs. It has been seen in order to estimate delay RC distributed models show 15% less error as compared to other.
17	V. Kumar, S. Rakheja and A. Naeemi /2013	IEEE International Symposium	Review of multi-layer graphene nanoribbons for on-chip interconnect applications	high frequency models, multi-conductor transmission lines, edge roughness	While comparing the performance of models, it was clear RC models was capable of predicting delay but error occurs while estimating frequency response. Thus MTL model is best suited for multilayer GNR to compute their frequency response for large range of frequencies in various RF applications.
18	W S. Zhao, W Y. Yin / 2014	IEEE Trans.	Comparative Study on Multilayer Graphene Nanoribbon (MLGNR) Interconnects	Crosstalk, Resistivity	It has been observed the advantages of MLGNR interconnects over Cu wires will not be degraded by the crosstalk effects.
19	M. Sahoo and H. Rahaman /2014	Fifth International Symposium on Electronic System Design (ISED)	Impact of line resistance variations on crosstalk delay and noise in multilayer graphene nano ribbon interconnects	Delay, noise, specular, Zigzag	Its well-known fact variation in various parameters have impact on performance of ML-GNR like interconnect width. MFP, dielectric thickness and constant. Delay performance is also affected by interlayer distance and doping concentration.
20	V R. Kumar, M K. Majumder, N R. Kukkam, B R. Kaushik / 2015	IEEE Trans.	Time and Frequency Domain Analysis of MLGNR Interconnects	Band width, Propagation Delay	Delay, bandwidth and power performances of Cu and doped MLGNR are compared using Equivalent single conductor (ESC) model. It has been seen the overall power dissipation and delay in doped MLGNR is significantly reduced by 43.72% and 86.13% respectively, in contrast with the Cu interconnects.
21	L. Qian, Y. Xia, G. Shi / 2016	IEEE Trans.	Study of crosstalk effect on the propagation characteristics of coupled MLGNR Interconnects	Crosstalk delay	In case of wider MLGNR interconnects the performance variation due the edge roughness is slightly less. As wire-length is linearly proportional to interconnect equivalent parasitics, there is increase in crosstalk delay with wire length. Also crosstalk delay is greater at out phase than at in-phase case because of Miller effect.

22	M G. Kumar, Y. Agarwal, R. Chandel / 2016	IETE Journal of Education	Carbon Nanotube Interconnects - A Promising Solution for VLSI Circuits	Crosstalk, Delay	The applications of MWCNT is seen in case of global interconnects, as they are mostly metallic and carry low resistivity compared with SWCNT bundle. MCB outperforms all structures of CNT as well as copper, providing reduction in propagation delay, crosstalk and power dissipation. Thus making MCB more efficient and best options for VLSI interconnects in future.
23	A. Alizadeh and R. Sarvari /2016	IEEE Trans.	Temperature-dependent comparison between delay of CNT and copper interconnects	Temperature, length, width	Variation in temperature can greatly have impact on parameters like length, width etc. GNRs outperform copper at various temperatures.
24	A K. Nishad, R. Sharma / 2016	IEEE Journal	Lithium-Intercalated Graphene Interconnects: Prospects for On-Chip Applications	Delay, Intercalation	Even if in case edge roughness is considered, optimized TC-MLGNR Li doped is regarded as fastest interconnect and shows very less delay and EDP, irrespective of local interconnect length among all other configurations. It has been, there is reduction in resistance with the increment in thickness of TC MLGNR interconnects.
25	J. Jiang, J. Kang, W. Cao, X. Xie, H.Zhang, J H. Chu, W. Liu, K. Banarjee /2016	Nano letters	Intercalation Doped Multilayer-Graphene-Nanoribbons for Next-Generation Interconnects	Contact resistance, Intercalation doping, Resistivity	Nevertheless by increased doping period the electrical conductivity of GNR is enhanced potentially but allowing it beyond a limited level can degrade over all GNRs conductivity by additional surface roughness and scattering.
26	S. Bhattacharya, D. Das, H. Rahaman / 2017	IETE Journal of Research	Stability Analysis in Top-Contact and Side-Contact Graphene Nanoribbon Interconnects	Stability	It is observed that by increasing the interconnect length (l) and width (w), the GM and PM increase. As a result, the relative stability increases. Copper-based interconnect shows more stability as compared to the TC-GNR and SC-GNR interconnect systems.
27	M G. Kumar, R. Chnadel, Y. Agarwal / 2017	IEEE Trans.	An Efficient Crosstalk Model For Coupled Multiwalled Carbon Nanotube Interconnects	Crosstalk, Electromigration	Also for 1000micrometer interconnect length peak-noise voltage is 6% greater in Cu as compared to MW-CNT interconnect. It can thus be concluded that very small latency is associated with MW-CNT interconnects.

28	Md. Al-Amin Howlader and M. A. G. Khan /2018	IEEE Conf.	Power Dissipation Analysis of Graphene Nanoribbon (GNR) Interconnects for Electronics in Nano Scale	Power dissipation, Heating system, resistance, delay	Analysis for power dissipation is conducted with varying layer number. MLGNR with 11 layers, low resistance and capacitance is seen. But talking about time delay and power dissipation it gets better with 15 layers. Thus MLGNR with 15 layers are suitable interconnects.
29	B. Kumari, M. Sahoo / 2018	IEEE Conf.	Width Optimization of Intercalation doped Multilayer Graphene Nanoribbon Interconnects	Crosstalk, Delay	Its investigated nearly and perfectly (p = 0.8 & 1 respectively) ML-GNR interconnects are most reliable and promising for future on chip VLSI interconnects.
30	W S. Zhao, Z H. Cheng, J. Wang, K. Fu, D W. Wang, P. Zhao, G. Wang, L. Dong / 2018	IEEE Trans.	Vertical Graphene Nanoribbon Interconnects at the End of the Roadmap	Propagation Delay, Resistivity	It is also observed that CNT and HGNR maintain better performance and are more reliable in contrast with copper. But thermal problems of HGNRs was a critical issue which was overcomed by VGNR

3.1 Comparison Table

Percentage reduction for doped MLGNR in power dissipation and propagation delay compared to copper [20].

Thickness (nm)	% reduction in propagation delay of MLGNR w.r.t Cu for interconnect lengths of			% reduction in power dissipation of MLGNR w.r.t Cu for interconnect lengths		
	100µm	500µm	1000µm	100µm	500µm	1000µm
5.75	88.01	89.79	90.11	49.39	50.61	54.04
11.50	85.13	88.97	89.61	50.93	52.98	57.17
17.25	83.78	88.44	89.42	51.12	54.17	59.14
23.00	81.91	87.98	89.27	51.32	55.82	60.61
28.75	80.05	87.53	89.15	51.47	57.31	61.21
34.50	78.46	87.10	89.04	51.57	58.02	61.57
40.25	77.11	86.67	88.92	51.66	58.99	61.72
46.00	75.76	86.25	88.82	51.69	60.13	61.81

3.2 Interconnect Properties

Interconnect properties of different materials [20]

Properties	**Cu**	**MWCNT**	**Graphene**
Max. current density (in A/cm^2)	10^7	10^9	10^9
Thermal conductivity (in 10^3 W/m-K)	0.385	3.0	3 - 5
Melting point (in K)	1356	3800	3800
Mean free path at room temperature (in nm)	40	2.510^4	10^3
Temperature coeff. Of resistance (10^{-3} /K)	4.0	-1.37	-1.47

4. Results and Discussions

According to the literature survey, it has been observed from the work that, copper has been the best interconnect material for more than a decade now and is still in use. However, as technology kept on moving down the nanoscale the issues with copper interconnects keeps on increasing in terms of current density, electromigration and mobility. There are several other materials other than copper, which were analyzed and compared to each other. It has been observed that graphene nanoribbons will be a promising candidate for future IC technology. By selecting a suitable material for interconnection, influence of various parameters like power dissipation, time delay, bandwidth and specularity can be further reduced to optimize the overall system performance. Also intercalation doped ML-GNR has been proved better candidate than any other possible candidate. Intercalation doping of ML-GNR remains open area of research. Using a proper material for intercalation can improve performance of overall parameters. The work has been done on several parameters like delay, noise, width, frequency, and crosstalk. But less work has been performed for optimizing geometric parameters in order to have least effect on crosstalk delay and power dissipation.

5. CONCLUSION

In conclusion, the various models were developed to predict the crosstalk in complicated VLSI design circuits. While performing scaling on various design parameters it's observed that there is increase in inductive noise. Unlike to that of resistive noise there is no change. Thus it poses a great challenge to have proper tradeoff between inductance and resistance. For replacement of issues in copper several forms of CNTs were analyzed. However, GNRs are considered future interconnects in nanoscale. ML-GNR has out powered copper in various ways. Intercalated ML-GNR has possibly low crosstalk delay than MCBs. Thus ML-GNRs can be analyzed further for future VLSI interconnects.

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